REMARKS

Claims 1-37 are pending. Independent Claims 1, 22, 26, 29 and 33 and dependent Claim 9 have been amended pursuant to the phone conversation with the Examiner on 14 Dec. 2004. No new matter has been added. The Examiner's reconsideration of the rejections is respectfully requested in view of the above amendments and the following remarks.

Support for the amendments made to the claims can for found within the specification as filed. For example, support can be found on pages 18 and 23 of the specification as filed.

Claim Rejections – 35 U.S.C. §102

In accordance with the Office Action, Claims 1-8, 15-20, 22, 23, 25-34 and 37 stand rejected under 35 U.S.C. §102(e), for reasons stated on pages 3-7 of the office action, as being anticipated by US Patent 6,678,790 to Kumar, hereinafter Kumar. Applicants respectfully submit that at the very minimum Kumar fails to anticipate Claims 1, 22, 26, 29, 30 and 33.

Applicants respectfully submit that at the very minimum Kumar does not teach or suggest a configurable memory comprising a memory portion for storing tag bits and data bits in a single data line in the memory portion, wherein the configurable memory is configured as a cache, as essentially claimed in Claim 1, 22, 26, 29, 30 and 33. Applicants further submit that by the present amendment, the term "logical line" has been changed to "data line in the memory portion". Logical is understood to mean a *logical* as opposed to a *physical line.*

In contrast, Kumar teaches in col. 3, lines 32-33, "...Each row of tag array 50 corresponds to one of the data lines in the data array 52...". By storing the tag bits and data bits in two different arrays, they are not stored in a single data line in the memory portion. Thus, Kumar fails to teach or suggest *a configurable memory comprising a memory portion for storing tag bits and data bits in a single data line in the memory portion, wherein the configurable memory is configured as a cache*, as essentially claimed in Claim 1, 22, 26, 29, 30 and 33.

Therefore Kumar fails to teach every element of Claim 1, 22, 26, 29, 30 and 33 and does not anticipate the above cited Claims fore at least the reasons stated above.

Applicants respectfully submit that at a minimum Claims 2-21, 23-25, 27, 28, 31, 32 and 34-37 are not anticipated by Kumar at least by virtue of their dependence from independent Claims 1, 22, 26, 29, 30 and 33 for at least the reasons stated above.

In accordance with the Office Action, Claims 1, 6, 9-14, 21 and 29 stand rejected under 35 U.S.C. §102(e), as being anticipated by US Patent 6,606,684 to Ramagopal et. al., hereinafter Ramagopal, for reasons cited on pages 6-8 of the Office Action. Applicants respectfully submit that at the very minimum, Ramagopal fails to anticipate Claims 1 and 29, since it does not teach or suggest *a configurable memory comprising a memory portion for storing tag bits and data bits in a single data line in the memory portion, wherein the configurable memory is configured as a cache* as essentially claimed in Claims 1 and 29.

In Contrast, Ramagopal, in col 3, lines 28-29, teaches the use of two super banks each of which can be configured as a cache or a SRAM. However, Ramagopal remains silent with regard to tag bits and data bits. Thus, Ramagopal fails to teach or suggest *a configurable memory comprising a memory portion for storing tag bits and data bits in a single data line in the memory portion, wherein the configurable memory is configured as a cache*, as essentially claimed in Claim 1 and 29.

Therefore Ramagopal fails to teach every element of Claim 1 and 29 and does not anticipate the above cited Claims.

Claims 6, 9-14 and 21 depend from Claim 1. The dependent claims are patentable over Ramagopal at least by virtue of their dependence from Claim 1.

With further regard to Claim 9, Applicants respectfully submit that Ramagopal fails to anticipate the claim for at least the following additional reason. Ramabopal does not teach or suggest a memory system *"... wherein the first mode of operation or the second mode of operation is selected during the program execution based upon comparing a supplied address to at least one address range contained in at least one configuration register..."*.

In contrast Ramagopal teaches in col. 4, lines 60-61, by "... monitoring certain bits in the physical memory address...". However, this is not the same as *comparing a supplied address to at least one address range contained in at least one configuration register* as is essentially claimed in Claim 9. Thus Ramagopal fails to teach every element of Applicants Claim 9 for at least the reasons stated above.

Therefore Ramagopal fails to anticipate the above cited Claims, for at least the reasons stated above.

In accordance with the Office Action, Claim 12 stands rejected under 35 U.S.C. §102(e), as being anticipated by US Patent 6,321,318 to Baltz, hereinafter Baltz, for the reasons given on pages 9-10 of the Office Action.

Applicants respectfully submit that at the very minimum, Baltz fails to anticipate Claim 1, from which claim 12 depends, because Baltz does not teach or suggest *a configurable memory comprising a memory portion for storing tag bits and data bits in a single data line in the memory portion, wherein the configurable memory is configured as a cache*, as essentially claimed in Claim 1.

In contrast, Baltz teaches, in the Abstract, a program memory controller that may comprise a tag RAM. This is not the same as the *a configurable memory comprising a memory portion for storing tag bits and data bits in a single data line in the memory portion* as essentially claimed in Claim 1, where a portion of the configurable memory is used to store tag bits and data bits, not the program memory controller as taught by Baltz.

Further still, by teaching that the memory controller comprises the tag RAM and not the program memory 31 Baltz again fails to teach *storing tag bits and data bits in a single data line in the memory portion* as is essentially claimed in Claim 1. By placing the tag RAM and the program memory in separate components, the tag bits and data bits could not possibly be on a single data line in the memory portion.

Thus, Baltz fails to teach every element of Claim 12 by virtue of its dependence form Claim 1 for at least the reasons given above.

Therefore Baltz fails to anticipate Claim 12.

Accordingly, withdrawal of the anticipation rejections is respectfully requested.

Claim Rejections – 35 U.S.C. §103

In accordance with the Office Action the following claim rejections were asserted under 35 U.S.C. §103(a):

(i) Claim 3 stands rejected as being unpatentable over Kumar in view of US Patent 6,355,968 to Lehmann, hereinafter Lehmann, for reasons stated on page 10 and 11;

(ii) Claim 24 stands rejected as being unpatentable over Kumar in view of US Patent 6,377,912 to Sample, hereinafter Sample, or in the alternative in view of US Patent 6,611,796 to Natarajan, hereinafter Natarajan, for the reasons stated on page 11 of the Office Action;

(iii) Claims 34 and 35 stand rejected as being unpatentable over Kumar in view of US Patent 6,426,549 to Isaak, hereinafter Isaak, for the reasons stated on pages 11-12 of the Office Action.

Each of the above rejections is based, in part, on the contention that Kumar teaches the elements of independent Claims 1, 22 and 33, from which Claims 3, 24, 34 and 35 respectfully depend. However, as Kumar, does not teach or suggest the inventions of Claims 1, 22 and 33 for the reasons discussed above. Because, none of the above cited references either alone or in combination cure the deficiencies of Kumar the above-cited references fail to establish a *prima facie* case for obviousness against any of the claimed inventions.

Accordingly, withdrawal of the obviousness rejections is respectfully requested.

All issues raised by the Examiner having been addressed, reconsideration of the rejections and an early and favorable allowance of this case is earnestly solicited.

Respectfully submitted,

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